a P-type base region that extends in said semiconductor substrate and defines a first P-N rectifying junction with the N-type drift region;

an N-type transition region that extends in said semiconductor substrate and defines a non-rectifying junction with the N-type drift region and a second P-N rectifying junction with said P-type base region;

an N+ source region that extends in said P-type base region and forms a third P-N rectifying junction with said P-type base region;

an insulated gate electrode that extends on said semiconductor substrate and is positioned opposite said P-type base region so that application of a sufficiently positive gate voltage to said insulated gate electrode causes formation of an inversion-layer channel that extends in said P-type base region and electrically connects said N+ source region to said N-type transition region;

a source electrode that is electrically coupled to said N+ source region;

a drain electrode that is electrically coupled to the N+ substrate region; and

means, comprising a trench-based insulated source electrode and P-type dopants in said P-type base region, for quickly depleting said N-type transition region in response to increases in a reverse bias across the second P-N rectifying junction so that when the N-type drift region switches from linear behavior to velocity saturated behavior the inversion-layer channel continues to sustain linear behavior and a maximum voltage at a drain side of the inversion layer channel is less than the positive gate voltage.

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